IN THE SPECIFICATION

On page 2, starting on line 11, please amend the paragraph as follows:

As shown in Fig. 1, in the LDMOS based on the conventional technique, the MOSFET is made on a wafer 13 which is constructed by P^- epitaxy layer 12 on P^+ substrate 11. What this is different from a general MOSFET device manufacturing process is that an overall lower part of the substrate is used as common source electrode 22 by forming a P^+ sinker 14 on a source side of the wafer 13 and connecting with a P^+ substrate 11.

On page 9, starting on line 24, please amend the paragraph as follows:

Fig. 3 is a structural sectional view of an HF power device taken along the line A-A′ of Fig. 2, and it is constructed by a P^- semiconductor layer 31b expitaxial-grown on a P^+ substrate 31a; a field oxide film 41 formed by a trench structure on one side of the P^- semiconductor layer 31b; a polysilicon 43a formed on a given surface of the P^- semiconductor layer 31b and gate electrode 44 of a tungsten silicide 43b laminating structure; a channel layer 46 laterally diffused from the field oxide film 41 to both sides of the gate electrode 44, and formed on the surface of the P^- semiconductor layer 31b; an N^+ source area 47 formed within the channel layer 46 between one side of the gate electrode 44 and the field oxide film 41; an N^+ drain area 48 formed on the surface of the P^- semiconductor layer 31b with a given interval from another side of the gate electrode 44; a P^+ sinker 37 provided as a column shape of a trench structure for dividing into two source areas by a piercing through the N^+ source area 47, and connected to the P^+ substrate 31a; an N^- LDD area 45 formed on the surface of the P^- semiconductor layer 31b between the N^+ drain area 48 and the gate electrode 44; source electrode 51 contacted with the N^+ source area 47 divided into two source areas and electrically coupled with the P^+ substrate 31a through the P^+ sinker 37; and drain electrode 52 contacted with the N^+ drain area 48.

On page 9, starting on line 23, please amend the paragraph as follows:

The P^- sinker 37 includes the P^+ polysilicon column 36b buried into one or numerous trenches formed by etching the P^- semiconductor layer 31b by a given depth